IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Tricomi et al.	**GROUP:**	2892
SERIAL NO:	10/531,141	**EXAMINER:**	Robert T. Huber
FILED:	August 29, 2005		
FOR:	SUPPORT DEVICE FOR MONOLITHICALLY INTEGRATED CIRCUITS		

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S BRIEF TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

PURSUANT TO 37 C.F.R. §§1.191 AND 41.37

Dear Sirs:

This appeal is in response to the Official Action dated November 24, 2009, and the Notice of Appeal filed in response thereto.

I hereby certify that this correspondence (along with any paper referred to as being attached or enclosed) is being transmitted electronically to the Commissioner for Patents via EFS-web, on the date indicated below.

Sarah L. Henry

Sarah L. Henry

5/24/10

Date

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I. REAL PARTY IN INTEREST

The real party of interest is Micronas GmbH of Freiburg, Germany.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF CLAIMS

A. Total number of Claims in the Application: 15

B. Status of All the Claims:

1) Claims cancelled: 1, 9–12

2) Claims withdrawn from consideration but not cancelled: 18–21

3) Claims pending: 2–8, 13–25

4) Claims allowed: None

5) Claims rejected: 2–8, 13–17, 22–25

6) Claims objected to: None

C. Claims on Appeal: 2–8, 13–17, 22–25

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Appellants provide each independent and dependent claim under appeal, and identify specific citations where support for each claim can be found within the specification, including the drawings. Support for each claim is not, however, limited to those specific citations and may also be found in additional areas of the specification and the drawings.

FEATURES OF CLAIM 2	SPECIFICATION
The integrated circuit of claim 16, wherein the stamped pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle.	Paragraphs: [0008] FIG: 1 Elements: α

FEATURES OF CLAIM 3	SPECIFICATION
The integrated circuit of claim 16, wherein the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device and each has an area for connection of a single bonding wire.	Paragraphs: [0007], [0009] FIG: 1–3

FEATURES OF CLAIM 4	SPECIFICATION
The integrated circuit of claim 16, wherein a height of each of the stamped pedestals lies in the range between 1/10 and 1.5 times of a height of the semiconductor die.	Paragraphs: [0017] FIG: 1

FEATURES OF CLAIM 5	SPECIFICATION
The integrated circuit of claim 16, wherein a height of each of the stamped pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device.	Paragraphs: [0017] FIG: 1

FEATURES OF CLAIM 6	SPECIFICATION
The integrated circuit of claim 16, wherein the stamped pedestals each represent a local deformation of the carrier device which is formed by a punch or a bending-off device.	Paragraphs: [0007], [0010], [0017] FIG: 1–3 Elements: 1, 2

FEATURES OF CLAIM 7	SPECIFICATION
The integrated circuit of claim 16, wherein the stamped pedestals are formed by application of material to the carrier device.	Paragraphs: [0010]

FEATURES OF CLAIM 8	SPECIFICATION
The integrated circuit of claim 16, wherein a silver or gold finish is applied to the stamped pedestals.	Paragraphs: [0011]

FEATURES OF CLAIM 13	SPECIFICATION
The integrated circuit of claim 17, where the stamped pedestals make an angle (α) greater than 45 degrees with the plane of the carrier device at all sidewalls, with the sidewalls having rounded junctions parallel to the plane of the carrier device or being rounded as a whole.	Paragraphs: [0008] Elements: α

FEATURES OF CLAIM 14	SPECIFICATION
The integrated circuit of claim 17, where the height of the stamped pedestals lies in the range between 1/10 of the die height and the die height itself.	Paragraphs: [0017] FIG: 1

FEATURES OF CLAIM 15	SPECIFICATION
The integrated circuit of claim 16, where only in the areas of the stamped pedestals, a finish, particularly silver or gold, is provided for bondability.	Paragraphs: [0003], [0011]

FEATURES OF CLAIM 16	SPECIFICATION
An integrated circuit, comprising:	Paragraphs: [0002]–[0006], [0017]–[0018] FIG: 1–3
a semiconductor die;	Paragraphs: [0002], [0006], [0007], [0017], [00018] FIG: 3 Elements: 7
a carrier device comprising a die paddle onto which the	Paragraphs: [0002], [0006], [0008],

die is attached,	[0011], [0017], [0018] FIG: 1–3 Elements: 1
where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle,	Paragraphs: [0006]–[0012] FIG: 1–3 Elements: 1, 2
where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;	Paragraphs: [0018] FIG: 2, 3 Elements: 1
a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion;	Paragraphs: [0018] FIG: 3 Elements: 8, 9, 10
a first bond wire extending from the die to a first of the plurality of stamped pedestals,	Paragraphs: [0017] FIG: 2, 3 Elements: 5, 6
and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion; and	Paragraphs: [0017], [0018] FIG: 3 Elements:5, 6, 8, 9, 10
a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.	Paragraphs: [0006]

FEATURES OF CLAIM 17	SPECIFICATION
An integrated circuit, comprising:	Paragraphs: [0002]–[0006], [0017]–[0018] FIG: 1–3
a semiconductor die;	Paragraphs: [0002], [0006], [0007], [0017], [00018] FIG: 3 Elements: 7
a metallic carrier device comprising a planar surface onto which the die is attached,	Paragraphs: [0002], [0006], [0008], [0011], [0017], [0018] FIG: 1–3 Elements: 1
where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface,	Paragraphs: [0006]–[0012] FIG: 1–3 Elements: 1, 2
where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;	Paragraphs: [0018] FIG: 2, 3

	Elements: 1
a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion; and	Paragraphs: [0017], [0018] FIG: 3 Elements:5, 6, 8, 9, 10
a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion.	Paragraphs: [0017], [0018] FIG: 2, 3 Elements:5, 6, 8, 9, 10

FEATURES OF CLAIM 22	SPECIFICATION
The integrated circuit of claim 16, where a height of at least one of the stamped pedestals is between 1/10 of a height of the carrier device to the height of the carrier device.	Paragraphs: [0007] FIG: 1

FEATURES OF CLAIM 23	SPECIFICATION
The integrated circuit of claim 17, where a height of at least one of the stamped pedestals is between 1/10 of a height of the metallic carrier device to the height of the metallic carrier device.	Paragraphs: [0007] FIG: 1

FEATURES OF CLAIM 24	SPECIFICATION
The integrated circuit of claim 16, where the metallic leads are separate from the carrier device.	Paragraphs: [0018] FIG: 3

FEATURES OF CLAIM 25	SPECIFICATION
The integrated circuit of claim 17, where the metallic leads are separate from the metallic carrier device.	Paragraphs: [0018] FIG: 3

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether claims 22 and 23 fail to comply with the written description requirement under the first paragraph of 35 U.S.C. § 112.

2. Whether claims 2–7, 13, 14, 16, 17, and 22–25 are obvious in view of the combined subject matter disclosed in U.S. Patent No. 5,479,050 to Pritchard et al. (hereinafter "Pritchard") and U.S. Patent No. 5,365,409 to Kwon et al. (hereinafter "Kwon").

3. Whether claims 8 and 15 are obvious in view of the combined subject matter disclosed in U.S. Patent No. 6,365,976 to Carter, Jr. et al (hereinafter "Carter") and Kwon.

VII. ARGUMENT

35 U.S.C. § 112 WRITTEN DESCRIPTION REJECTION

DEPENDENT CLAIM 22

Dependent claim 22 recites the integrated circuit of claim 16, where a height of at least one of the stamped pedestals is between 1/10 of a height of the carrier device to the height of the carrier device. The Official Action dated November 24, 2009 (hereinafter "the Official Action") contends that the claimed subject matter fails to comply with the written description requirement under the first paragraph of 35 U.S.C. § 112. Appellants respectfully disagree.

The Official Action contends that "*the claim(s) contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.*" (Official Action, pg. 2) Specifically, the Official Action contends that "*the claims recite 'a height of at least one of the stamped pedestals is between 1/10 of a height of the carrier device to the height of the carrier device'*" and that "*there is no support in the specification for such a limitation*". (Official Action, pg. 2) The Official Action argues that the specification supports only pedestal heights that "*may be approximately in a range of from 1/5 to twice the material thickness h of the carrier device*". (Official Action, pg. 2–3)

Appellants respectfully direct the Board to paragraph [0007] of the specification, which discloses that *"[i]f the raised pedestal is formed by a drawing or pressing process during the manufacture of the frame using a punchlike tool, the height will range from about 1/10 of the material thickness of the carrier to the carrier thickness itself.*" For at least this reason, Appellants respectfully submit that claim 22 fully complies with the written description

requirement under the first paragraph of 35 U.S.C. § 112, and request that this rejection be withdrawn.

DEPENDENT CLAIM 23

Dependent claim 23 recites the integrated circuit of claim 17, where a height of at least one of the stamped pedestals is between 1/10 of a height of the metallic carrier device to the height of the metallic carrier device. The Official Action contends that the claimed subject matter fails to comply with the written description requirement under the first paragraph of 35 U.S.C. § 112. Appellants respectfully disagree. Appellants respectfully submit that claim 23 is supported by the necessary written description for at least the reasons as set forth above with respect to claim 22, and request that this rejection be withdrawn.

35 U.S.C. §103(A) OBVIOUSNESS REJECTIONS

1. REGARDING THE COMBINATION OF PRITCHARD AND KWON

INDEPENDENT CLAIM 16

Independent claim 16 recites an integrated circuit, comprising:

> a semiconductor die;
> a carrier device comprising a die paddle onto which the die is attached, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle, where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;
> **a plurality of metallic leads** each comprising an inner lead portion that extends to an outer lead portion;
> a first bond wire extending from the die to a first of the plurality of stamped pedestals, and **a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion**; and
> **a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions**.

(cl. 16, emphasis added). The Official Action contends that a person of ordinary skill in the art would have been motivated to combine the teachings of Pritchard and Kwon to make such an integrated circuit. Appellants respectfully disagree.

The Official Action acknowledges that Pritchard fails to teach or suggest "*that the plurality of leads are metallic, the second bond wire extends from the first of the plurality of stamped pedestals to the inner lead portion, and a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.*" (Official Action, pg. 4–5). Thereafter, the Official Action contends that "*Kwon discloses an integrated circuit structure (e.g. figure 5), comprising a first bond wire (bond wire 160) extending from the die (die 154) to a first of the plurality of pedestals (pedestals 158), and a second bond wire (bond wire 162) extending from the first of the plurality of pedestals to an inner lead portion (inner lead portion of lead 156); and a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions (e.g. as seen in figure 5, there is a package, denoted by a dashed line, that encapsulates the die, paddle wires and inner lead portions).*" (Official Action, pg. 5). Finally, the Official Action concludes that "*[i]t would have been obvious for one of ordinary skill in the art at the time the invention was made to modify the device in Pritchard such that the second bond wire extends from the stamped pedestal to the inner lead portion since Pritchard discloses that electrical connections may be formed between the die, pedestals, and surrounding leads, and Kwon discloses that connections between pedestals and surround leads can be made.*" (Official Action, pg. 5).

Appellants respectfully submit that neither Pritchard nor Kwon are being properly considered as a whole. *See, e.g., In re Wesslau*, 353 F.2d 238, 241 (C.C.P.A. 1965) ("*It is impermissible within the framework of section 103 to pick and choose from any one reference only as much of it as will support a given position, to the exclusion of other parts necessary to the full appreciation of what such reference fairly suggests to one of ordinary skill in the art*"); *see also* Chisum on Patents 5.03(F) ("*The court asserted that a single line in a prior art*

reference should not be taken out of context and relied upon with the benefit of hindsight to show obviousness. Rather, a reference should be considered as a whole, and portions arguing against or teaching away from the claimed invention must be considered") (referring to the holding in *Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc.*, 796 F.2d 443 (Fed. Cir. 1986)).

First, Pritchard teaches, as illustrated in FIGS. 1 to 3, that "*[b]ridges 12 and 13 are stamped from a part of die mount pad 16 . . . .*" (Pritchard, col. 1, line 67 to col. 2, line 1). "*Ground wires are bonded to the tops (12a and 13a) of the pedestals* [i.e., the bridges 12 and 13] *by wires 14 and 15. Connections to the die are made to ground pads on the die.*" (Pritchard, col. 2, lines 12-15). "*At two ends of die 33 are raised pedestals 23 and 25 formed from the surface of die mount pad 21. Bridges, and therefore die mount pad 21, are electrically connected to die 33 by wires 24 and 26.*" (Pritchard, col. 2, lines 28-31). Further, as illustrated in FIG. 2, the die mount pad 21 is directly coupled to two sets of leads on opposing ends of the die mount pad 21. Thus, according to a fair and proper reading, Pritchard teaches electrically connecting the ground pads on the die 11 (FIG. 1) to the two sets of grounding leads directly coupled to the die mount pad 21 (FIG. 2). That is, the ground wires 14, 15 connect the ground pads on the die 11 to the pedestals / bridges 12, 13. The pedestals / bridges 12, 13 are interconnected with the die mount pad 21, which is connected to the grounding leads. (Pritchard, FIGs. 1 and 2). Notably, according to a fair and proper reading of Pritchard, this direct connection between the grounding leads and the ground wires 14, 15 via pedestals 12, 13 may prevent bond destruction during temperature cycling and thermal shock. (Pritchard, col. 1, lines 35-45).

As a result of the foregoing, Pritchard teaches away from incorporating the bonding wires 162 as taught in Kwon (Kwon, FIG. 5) to connect the pedestals 12, 13 to the grounding leads or leads 17, 18 in Pritchard. (A) The bonding wires 162 connecting the interposers/traces 158 to the

bonding fingers 156 as taught in Kwon would negate the limitation of the direct connection between the pedestals 12, 13 and the grounding leads coupled to the die mount pad 21 as taught in Pritchard. That is, the electrical connection between the stamped pedestals 12, 13 and the grounding leads through the die mount pad 21 would become redundant. (B) Pritchard explicitly teaches away from the addition of the bonding wires 162 as taught in Kwon since such wires may fracture and sag during temperature cycling and thermal shock, whereas the single structural connection between the grounding wires 14, 15 and the grounding leads via the bonding pad 21 as taught in Pritchard may prevent such destruction. (Pritchard, col. 1, lines 13-33 and lines 35-45).

Second, as set forth above, according to a fair and proper reading of Pritchard as a whole, the tops of the pedestals, the raised pedestals themselves, the die mount pad and the die are electrically interconnected, where the pedestals are formed by stamping the die mount pad. (Pritchard, col. 1, line 62 to col. 2, line 38). In contrast, according to a fair and proper reading of Kwon as a whole, the bonding pad 102, 152 is electrically isolated from the traces/interposers 110, 158 (which the Action equates to the pedestals in Pritchard), the leads 106, 156, and the die 104, 154. (Kwon, col. 5, line 57 to col. 6, line 50). Further, as illustrated in FIGS. 4 and 5, the bonding pad 102, 152 and the traces/interposers 110, 158 are each separate and distinct elements. (Kwon, col. 5, line 57 to col. 6, line 50). Specifically, Kwon teaches that the integrated-circuit package 100, 150 "*uses an **electrically-insulated**, heat-conducting substrate 102 **as a bonding pad** for an integrated-circuit die 104. The electrically-insulated, heat-conducting substrate 102 is formed of a ceramic material such as alumina nitride, beryllium oxide, a very thin polymeric film, on an equivalent material having good heat conduction characteristics.*" (Kwon, col. 5, lines 57-65, emphasis added).

As a result, Kwon teaches away from the electrically interconnected pedestals as taught in Pritchard. Specifically, Pritchard teaches that the pedestals 12, 13 are electrically connected to the die mount pad 21 which, according to a fair and proper reading, is electrically connected to the grounding leads. (Pritchard, col. 1, line 62 to col. 2, line 38). In contrast, Kwon teaches using the bonding wires to connect the electrically insulated (i.e. non-electrically connected) traces/interposers 110, 158 and bonding fingers 156. (Kwon, col. 5, line 57 to col. 6, line 50).

The foregoing arguments were presented to the Examiner in an Amendment dated August 5, 2010. In response to Appellants arguments, the Examiner summarily rejected Appellants arguments on two grounds.

First, the Examiner rejected Appellants' reasoning that Pritchard teaches away from connecting the pedestals to the leads because the wires may fracture and sag during temperature cycling and thermal shock. The Examiner argued that Pritchard discloses that the wires connecting the semiconductor die to the raised pedestal are done such that the wires "*will not sag and contact the die in an undesirable location*" and that "*this [] does NOT preclude the connection of the pedestals to the surrounding leads by a wire bond.*" (Official Action, pg. 15) The Examiner then cited FIG. 1 and wire bonds 2 to support his conclusion that Pritchard shows that there indeed may be wire bonds directly connected to the surrounding leads. (Official Action, pg. 15). Appellants respectfully disagree with the Examiner's characterization of Pritchard. Specifically, Appellants submit that the one of the primary objects of the invention disclosed in Pritchard is to prevent any and all sagging of bond wires—not just sagging of bond wires that may result in unwanted contact of the wires with the die. (Pritchard, col. 1, lines 41–44). As such, Appellants submit that Pritchard teaches away from connecting the pedestals to the leads, because doing so would necessitate the use of bond wires of substantially greater

length than bond wires 14, 15 (which are used to connect the ground pads on the die 11 to the pedestals / bridges 12, 13) and bond wires 20, 22 (which are used to connect the ends of the lead frame fingers and bond pads 19, 21 on die 11). The use of longer bond wires to connect the pedestals to the leads would inevitably increase the likelihood of sagging of bond wires and destruction of the bond during temperate cycling and thermal shock.

Second, the Examiner rejected Appellants reasoning that Kwon teaches away from electrically interconnecting the pedestals because the integrated circuit package integrated circuit package 100, 150 "*uses an electrically-insulated, heat-conducting substrate 102 as a bonding pad for an integrated-circuit die 104.*" (Kwon, col. 5, lines 59–61). The Examiner argues that the properties of the substrate is not germane to the teaching relied upon for the combination of Kwon with Pritchard. (Official Action, pg. 15–16) The Examiner argues that it is the connection of the leads to the pedestals of Kwon that is used to modify the device of Pritchard, and not the material of the substrate. (Official Action, pg. 15–16) Appellants respectfully disagree with the Examiner's characterization of Kwon. Specifically, Appellants submit that the properties of the substrate are in fact germane to the teaching.

To best understand Appellants reasoning, Appellants direct the Board to the Background of the Invention portion of the instant application, which provides: "*The reference potential of a monolithic integrated circuit, usually ground potential or a supply potential, should be uniform and undisturbed. To accomplish this in the best possible manner under all operating conditions, most monolithic integrated circuits are connected to the reference potential not only via their backside and the carrier platform, but the circuit itself is connected to the carrier platform via a plurality of additional connections. This is commonly done by providing bonding wires between bonding pads on the chip surface and the carrier platform.*" (¶ [0003], emphasis added). Based

on the foregoing principle, the connection of the pedestals to the leads in the present application serves to create a uniform and undisturbed ground potential or supply potential between the chip, the leads, *and* the carrier platform. In contrast, in Kwon, the connection of the leads to the pedestals serves to create a uniform and undisturbed ground potential or supply potential *only* between the chip and the leads. Because the carrier platform in Kwon is an electrically-insulated, heat-conducting ceramic substrate 152, there is no reason to ground the carrier platform and thus no reason to provide bonding wires between the bonding pads on the chip surface and the carrier platform. In fact, Kwon makes clear that the multiple bond wires 112, 116 and interposers 158 are employed only to enable use of dies of various sizes. (col. 1, lines 51–68)

For at least these reasons, it is submitted that a person of ordinary skill in the art would not have been motivated to combine the teachings of Pritchard and Kwon as the two references respectively teach away from each other. Therefore, Appellants respectfully submit that claim 16 is not obvious in view of Pritchard and Kwon, and request that this rejection be withdrawn.

As a result, Appellants respectfully submit that claim 16 is patentable over the combination of Pritchard and Kwon.

INDEPENDENT CLAIM 17

Independent claim 17 recites an integrated circuit comprising:

> a semiconductor die;
> a metallic carrier device comprising a planar surface onto which the die is attached, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface, where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;
> **a plurality of metallic leads** each comprising an inner lead portion that extends to an outer lead portion; and
> a first bond wire extending from the die to a first of the plurality of stamped pedestals, and **a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion**.

(cl. 17, emphasis added). The Official Action contends that a person of ordinary skill in the art would have been motivated to combine the teachings of Pritchard and Kwon to make such an integrated circuit. Appellants respectfully submit that claim 17 is patentable for at least the reasons as set forth above with respect to claim 16. Specifically, a person of ordinary skill in the art would not have been motivated to combine the teachings of Pritchard and Kwon as the two references respectively teach away from each other.

DEPENDENT CLAIMS 1–7, 13–14, 22– 25

Appellants respectfully submit that these rejections are moot since claims 16 and 17 are patentable for at least the reasons as set forth above.

2. REGARDING THE COMBINATION OF CARTER AND KWON

DEPENDENT CLAIMS 8 AND 15

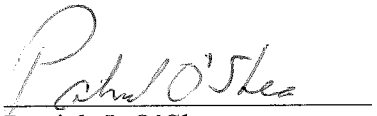
Appellants respectfully submit that these rejections are moot since claims 16 and 17 are patentable for at least the reasons as set forth above.

VIII. CONCLUSION

For all the foregoing reasons, Appellants submit that the rejection of claims 2–8, 13–17, 22–25 is erroneous and reversal thereof is respectfully requested.

If there are any additional fees due in connection with the filing of this appeal brief, please charge them to our Deposit Account No. 50-3381.

Respectfully submitted,



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CLAIMS APPENDIX

2. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals have sidewalls with an angle (α) greater than 45 degrees with respect to a plane of the carrier device die paddle.

3. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals each have a plane surface which is parallel to a chip connection area plane of the carrier device and each has an area for connection of a single bonding wire.

4. (Previously Presented) The integrated circuit of claim 16, wherein a height of each of the stamped pedestals lies in the range between 1/10 and 1.5 times of a height of the semiconductor die.

5. (Previously Presented) The integrated circuit of claim 16, wherein a height of each of the stamped pedestals lies in the range from 1/5 to twice a material thickness (h) of the carrier device.

6. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals each represent a local deformation of the carrier device which is formed by a punch or a bending-off device.

7. (Previously Presented) The integrated circuit of claim 16, wherein the stamped pedestals are formed by application of material to the carrier device.

8. (Previously Presented) The integrated circuit of claim 16, wherein a silver or gold finish is applied to the stamped pedestals.

13. (Previously Presented) The integrated circuit of claim 17, where the stamped pedestals make an angle (α) greater than 45 degrees with the plane of the carrier device at all sidewalls, with the sidewalls having rounded junctions parallel to the plane of the carrier device or being rounded as a whole.

14. (Previously Presented) The integrated circuit of claim 17, where the height of the stamped pedestals lies in the range between 1/10 of the die height and the die height itself.

15. (Previously Presented) The integrated circuit of claim 16, where only in the areas of the stamped pedestals, a finish, particularly silver or gold, is provided for bondability.

16. (Previously Presented) An integrated circuit, comprising:

a semiconductor die;

a carrier device comprising a die paddle onto which the die is attached, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the die paddle, where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;

a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion;

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion; and

a package that encapsulates the semiconductor die, the die paddle, the first and second bond wires and the inner lead portions.

17. (Previously Presented) An integrated circuit, comprising:

a semiconductor die;

a metallic carrier device comprising a planar surface onto which the die is attached, where a plurality of stamped pedestals are arranged on the carrier device exteriorly surrounding and adjacent to the planar surface, where the carrier device, the die paddle and the stamped pedestals form a single piece unitary structure;

a plurality of metallic leads each comprising an inner lead portion that extends to an outer lead portion; and

a first bond wire extending from the die to a first of the plurality of stamped pedestals, and a second bond wire extending from the first of the plurality of stamped pedestals to an inner lead portion.

22. (Previously Presented) The integrated circuit of claim 16, where a height of at least one of the stamped pedestals is between 1/10 of a height of the carrier device to the height of the carrier device.

23. (Previously Presented) The integrated circuit of claim 17, where a height of at least one of the stamped pedestals is between 1/10 of a height of the metallic carrier device to the height of the metallic carrier device.

24. (Previously Presented) The integrated circuit of claim 16, where the metallic leads are separate from the carrier device.

25. (Previously Presented) The integrated circuit of claim 17, where the metallic leads are separate from the metallic carrier device.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.